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This paper explains how non-volatile memory (NVM) devices with an oxide/nitride/oxynitride (ONO) structure on a rough poly-silicon (poly-Si) surface were fabricated and studied using poly-Si thin film transistor (TFT) technology on a glass substrate. When a flat panel display (FPD) such as an organic light emitting diode (OLED) or a liquid crystal device (LCD) displays a static image, the brightness of the panel is altered because of degradation of the driving current. In order to prevent degradation of the driving current, an NVM device can be applied to the compensation circuit for the pixels of a FPD. To fabricate an NVM device on glass, a metal/oxide/nitride/oxynitride/poly-Si (MONOS) structure with an ultra-thin silicon oxynitride (SiOxNy) using nitrous oxide (N_2O) plasma as the tunneling layer was used instead of the general methods of oxidation and deposition for ultra-thin silicon dioxide (SiO_2). The memory window of a fabricated NVM device which has a MONOS structure with a tunneling layer of ultra-thin SiOxNy at a programming voltage of $-16\,V$ and erasing voltage of $+11\,V$ for a pulse time of 1s is 2.8 V. This is because of programming and erasure of charges in the silicon nitride (SiNx) layer. Because of the properties of NVM device on glass, NVM devices can be used in various FPD.

Keywords: nitrous oxide (N_2O); nonvolatile memory (NVM); oxide/nitride/oxynitride (ONO); plasma-assisted oxynitridation; poly-silicon (poly-Si)

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INTRODUCTION

Low temperature poly-Si (LTPS) TFTs have been the subject of extensive research in the last few years. This is because of various advantages, such as high mobility and good applicability of functional circuits for FPDs [1,2]. For applications such as system-on-panel (SOP), additional functional devices on glass have been fabricated. The low power consumption is the most important factor for various SOP applications. Recently, FPDs with built-in NVM devices have attracted substantial interest [3–5]. When FPDs such as OLED and LCD display static images, the power consumption is increased and the brightness of panel is altered due to degradation of the driving current. In order to prevent degradation of the driving current, an NVM device can be applied to the compensation circuit for the pixels of an FPD. This paper investigates the applicability of memory in pixel (MIP) type NVM devices on a glass substrate for SOP applications.

Various crystallization methods such as ELA, solid phase crystallization (SPC), and metal induced crystallization (MIC) have been used for fabricating poly-Si thin film. The main disadvantages of SPC and MIC methods are that they are difficult to apply in a glass substrate with a large area because of high crystallization temperatures and the existence of metal residues in poly-Si after crystallization. ELA is the most suitable method for achieving large area poly-Si on glass in poly-Si TFT manufacturing, because of the high quality of poly-Si and low temperature process for the creation of poly-Si [6]. After a short period of laser irradiation, the high surface roughness is found to be caused by the melting/crystallization of a-Si. General thermal oxidation and deposition methods cannot create a uniform ultra-thin tunneling layer on rough poly-Si for NVM devices. However Chen et al. [7,8] reported the fabrication of NVM on poly-Si using a planarization procedure and position control during laser irradiation on a-Si surface for crystallization. In some cases, plasma-assisted oxidation and nitridation, [9,10] is used for the deposition of uniform ultra-thin films. For this method, plasma-assisted oxynitridation is applied to form a uniform tunneling layer instead of the conventional oxidation and deposition methods. This is because the planarization procedure is not suitable for currently practical semiconductor processing. In our previous work [11], we demonstrated the efficiency of a silicon oxynitride layer using plasma-assisted oxynitridation as the tunneling layer for an NVM device. Silicon oxynitride films have properties which make them a better gate dielectric suitable to replace silicon dioxide in submicron TFTs and as the tunneling layer of NVM devices. For the fabrication of the NVM device on glass, an ONO stack

structure was used as a gate insulator to enable charge trapping and retention. The characteristics of the NVM device with the ONO stack structure on glass were investigated.

EXPERIMENTAL

A cross-sectional view of the poly-Si NVM device on glass is shown in Figure 1. On the glass substrates, $SiNx/SiO_2$ buffer layers were deposited with 200 nm/100 nm thickness, respectively. After buffer layers deposition, a 50 nm thick a-Si film was deposited by plasma CVD. To crystallize a-Si, the a-Si film was treated at an energy density of 300 mJ/cm^2 using a 308 nm XeCl laser. After the formation of poly-Si, the ultra-thin SiOxNy film which forms the tunneling layer was deposited by plasma at a substrate temperature of 350°C and radio frequency (RF) power of 150 W, respectively. During plasma-assisted oxynitridation of poly-Si surface, only N_2O as a reactant gas was used. An Aluminum electrode with an area 4.91×10^{-8} m^2 was formed for the MOS capacitor by evaporation. Subsequent to this the high frequency (1 MHz) capacitance-voltage (C-V) characteristics of the MOS with ultra-thin SiOxNy as insulator layer were investigated. Subsequent to this, the ONO stack structure was formed using 2.7 nm thick SiOxNy as a tunneling layer, 35 nm thick SiNx as a charge trapping layer, and 12.5 nm thick SiO_2 as a blocking layer. The thickness of each thin film was measured by an ellipsometer using 1.95 eV light. After the deposition of a gate metal, the sample was patterned and doped by the boron ion shower method for the source and drain regions. After the fabrication of poly-Si NVM devices on glass, the devices were examined to evaluate the electrical memory properties.

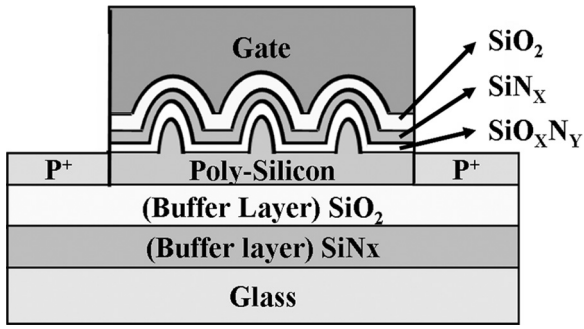

FIGURE 1 A cross-sectional view of the poly-Si NVM device with ONO stack structure on glass substrate.

The switching properties of a poly-Si NVM device on glass were measured by using the shift of threshold voltage of transfer characteristics. The transfer properties of the poly-Si NVM devices were measured at room temperature where $V_{DS} = -1\,V$.

RESULTS AND DISCUSSION

The thickness and refractive index of ultra-thin SiOxNy films versus plasma treatment time is shown in Figure 2. To establish the optimal thickness for the growth of the ultra-thin SiOxNy layer to use as a tunneling layer for a MONOS memory device, ultra-thin SiOxNy layers were deposited by varying the N_2O plasma treatment time under optimal RF power of 150 W. The N_2O flow rate and substrate temperature were fixed at 2.5 sccm and 350°C, respectively for all the samples. Plasma-assisted oxynitridation was implemented for different treatment times which varied from 1 to 30 min. The thickness and refractive index of SiOxNy films was gradually increased and saturation occurred at a thickness of 2.7 nm and a refractive index of 1.65. This is because of the penetration limit of oxygen and nitrogen during a plasma-assisted oxynitridation procedure. The ultra-thin SiOxNy films have the refractive index ($n \sim 1.65$) between stoichiometric SiO_2 ($n \sim 1.45$) and SiNx ($n \sim 2.05$) because SiOxNy film is regarded as a physical combination of two distinct phases formed by SiO_2 and SiNx.

Properties of the MOS structure with a SiOxNy layer as insulator were studied by using C-V as shown in Figure 3. The characteristic

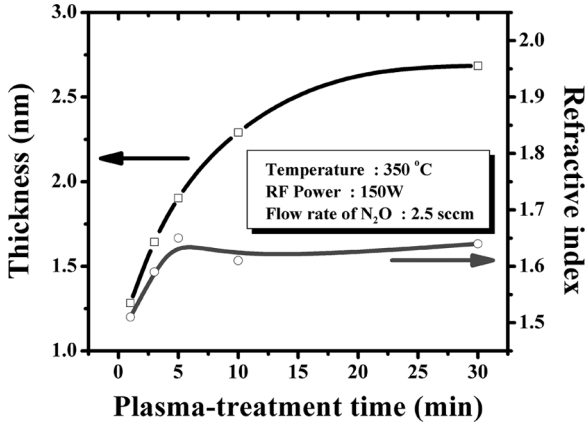

FIGURE 2 The thickness and refractive index of ultra-thin SiOxNy films versus N_2O plasma treatment time.

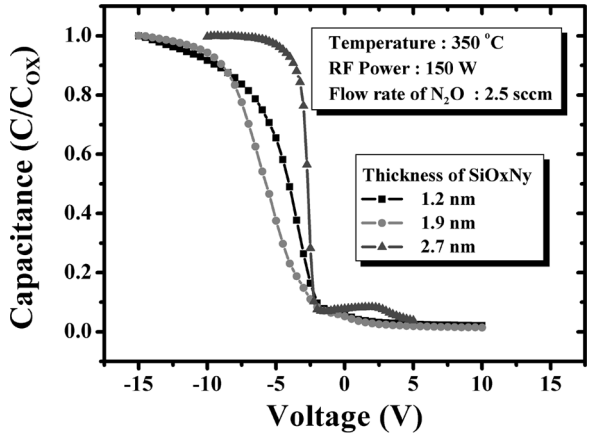

FIGURE 3 The C-V properties of MOS structures using ultra-thin SiOxNy films grown with different plasma treatment times as a gate insulator. The electrical C-V measurements are performed by voltage sweep from inversion (+V) to accumulation (−V).

C-V curves of MOS structures fabricated by using a SiOxNy layer deposited with a plasma treatment time of 30 min shows a clear separation between inversion and accumulation regions, implying that the ultra-thin SiOxNy layer is applicable to the fabrication of poly-Si TFT and NVM device. The characteristic C-V curves of MOS structures fabricated by using a SiOxNy layer deposited with plasma treatment times of less than 5 min, however, show an unstable accumulation region due to a very thin oxynitrided layer. In order to demonstrate the stability of SiOxNy film deposited with a plasma treatment time of 30 min, stress measurement was carried out, as shown in Figure 4. After the MOS structure with ultra-thin SiOxNy film as insulator layer was biased using a stress voltage of ± 10 V for 1 min at a gate electrode, the C-V characteristics of the MOS were established. No large variation of the C-V curve due to charge trapping in SiOxNy films or at the interface between Si and SiOxNy was observed. Although the thickness of SiOxNy film is less than 3 nm, the ultra-thin SiOxNy film does not suffer breakdown during a bias voltage of ± 10 V and biasing time of 1 min. The ultra-thin SiOxNy film formed by using N_2O plasma treatment reported in this paper can be used for the fabrication of TFT and as a tunneling layer for an NVM device.

The Programming/Erasure properties of poly-Si NVM devices with an ONO stack structure on glass were evaluated by measuring the

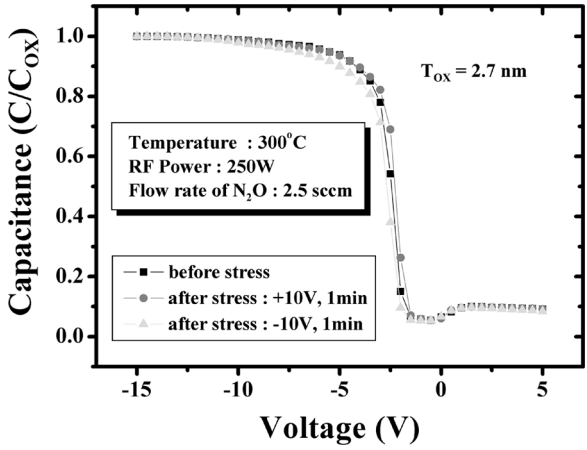

FIGURE 4 The C-V properties of MOS structures for the stability test of SiOxNy film deposited with a plasma treatment time of 30 min. The condition used is a stress voltage of ± 10 V for 1 min at a gate electrode.

threshold voltage shift for transfer properties. The transfer properties of a poly-Si NVM device with an ONO stack on glass after programming are shown in Figure 5. The length and width of the NVM device were 16 μm and 16 μm, respectively. The devices were programmed by applying a negative gate voltage from -16 V to -20 V in intervals of -1 V for a programming pulse time of 1 s to the control gate where $V_S = V_D = 0$, respectively. When a gate voltage of more than -16 V is applied to the poly-Si NVM device with the MONOS structure on glass, the holes tunnel from the valence band of the poly-Si through the tunneling oxynitride film and are trapped in the forbidden gap of the nitride layer. Consequently, the threshold voltage is shifted towards negative voltage. The transfer properties of the poly-Si NVM device with the ONO stack on glass after erasure are shown in Figure 6. The length and width of the NVM device were 16 μm and 16 μm, respectively. The devices were erased by applying a positive gate voltage from $+9$ V to $+14$ V in intervals of 1 V for an erasure pulse time of 1s to the control gate where $V_S = V_D = 0$, respectively. When a gate voltage of more than $+9$ V is applied to the device, the electrons tunnel from the poly-Si through the tunneling oxynitride film. The holes either recombine with the electrons trapped in the nitride layer or the trapped holes may be emitted from the trapped state to the channel. It can be seen from Figures 5 and 6 that the threshold voltage shift is -1.1 V at a programming voltage of -16 V and programming pulse time of 1 s. The threshold voltage shift is more

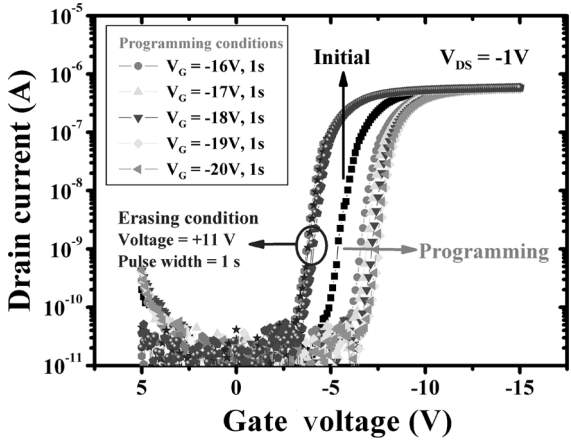

FIGURE 5 The transfer properties of poly-Si NVM with an ONO stack structure on glass after programming. The programming condition used is a gate bias from $-16\,V$ to $-20\,V$ in intervals of $-1\,V$ for a programming pulse time of 1 s, where $V_S = V_D = 0$.

than 1.7 V at an erasure voltage of more than $+11\,V$ and an erasure pulse time of more than 1 s. The difference of the threshold voltage shift is large enough to define the "0" or "1" state for a logic memory circuit.

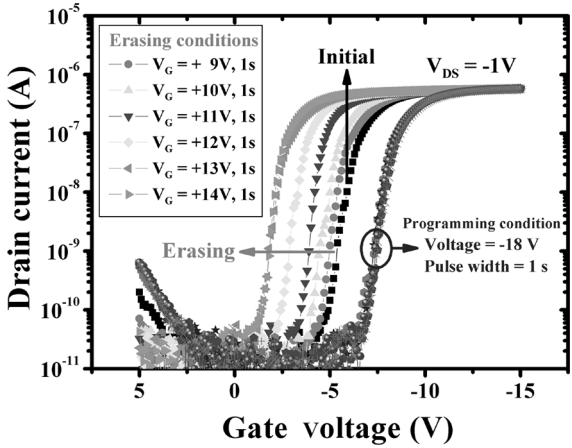

FIGURE 6 The transfer properties of poly-Si NVM with an ONO stack structure on glass after erasure. The erasure condition used is a gate bias from $+9\,V$ to $+14\,V$ in intervals of $+1\,V$ for an erasure pulse time of 1 s, where $V_S = V_D = 0$.

CONCLUSIONS

In this paper, poly-Si NVM devices were fabricated and studied which have an ONO stack structure on poly-Si with a rough surface formed using ELA on glass. In order to fabricate the NVM devices on glass, plasma-assisted oxynitridation is applied to form a uniform tunneling layer on poly-Si with a very rough surface. The charge storage of the poly-Si NVM device on glass was confirmed by measuring the threshold voltage shift for the transfer properties. The threshold voltage shift increased as the voltage and pulse time used for programming and erasure were increased. The memory window of a fabricated NVM device with a MONOS structure which has a tunneling layer of ultra-thin SiOxNy at a programming voltage of -16 V and an erasure voltage of $+11$ V for a pulse time of 1 s is 2.8 V. This is because of the programming and erasure of charges in SiNx. The characteristics of the poly-Si NVM device on glass could be improved for future applications by optimizing the conditions.

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